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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/060,750	01/30/2002	Robert J. Devins	BUR9-2001-0016-US1	7058
29154 7590 03/03/2009 FREDERICK W. GIBB, III Gibb Intellectual Property Law Firm, LLC 2568-A RIVA ROAD SUITE 304 ANNAPOLIS, MD 21401			EXAMINER GUILL, RUSSELL L	
			ART UNIT 2123	PAPER NUMBER
			MAIL DATE 03/03/2009	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<p align="center"><b>Advisory Action</b> <b>Before the Filing of an Appeal Brief</b></p>	<p><b>Application No.</b> 10/060,750</p>	<p><b>Applicant(s)</b> DEVINS ET AL.</p>	
	<p><b>Examiner</b> Russ Guill</p>	<p><b>Art Unit</b> 2123</p>	

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 17 February 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☐ The period for reply expires \_\_\_\_\_ months from the mailing date of the final rejection.  
b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: 2,8-27.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.  
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). \_\_\_\_\_.  
13. ☐ Other: \_\_\_\_\_.

/Paul L Rodriguez/  
Supervisory Patent Examiner, Art Unit 2123

Continuation of 11. does NOT place the application in condition for allowance because:  
While the Examiner appreciates the Applicant's arguments, the Examiner respectfully disagrees, as follows.

The following principle applies: Substantial evidence is evidence that "a reasonable mind might accept as adequate to support a conclusion. In re Gartside, 203 F.3d 1305 (Fed. Cir. 2000).

Regarding claims 2, 8-27 rejected under 35 U.S.C. § 112, first paragraph:

Applicant's arguments appear to be the same arguments that were made in the previous response, thus the response from the Final Office action is repeated below.

The argument recites, "A system-on-a chip (SOC) comprises a number of logic blocks, also called "cores", which are integrated into a single silicon device". While an SOC may be a silicon device, the specification appears to be directed to a software SOC. As discussed in paragraphs [0001] – [0008] of the specification, an SOC may be interpreted as software. Also, see paragraph [0025] which recites, "Figure 2 shows a computer system which can be used to implement the present invention", which appears to imply that the invention is not a hardware SOC, since the invention is implemented on a computer with a simulator. Since the preceding arguments are also used below for the rejections under 35 U.S.C. § 101, the Examiner remarks that if a claim has both statutory and non-statutory interpretations, the claim must be amended to have only a statutory interpretation. If the SOC is hardware, then the claims should be amended to indicate this. If the SOC is software, then the claims should be amended to include hardware.

The argument recites, "i.e., a structure (i.e., hardware) that attaches an external model (i.e., hardware) to a SOC interface (i.e., hardware) and to an external bus interface unit (i.e., hardware)". The Examiner respectfully disagrees with the interpretation, as follows.

(1) The recited structure ("a structure (i.e., hardware)"), appears to be a software structure (see specification paragraph [0019], "an SOC structure 300 (e.g., a verification test bench)", where the verification test bench is software as shown at least in figure 2, element 450; and see specification, paragraph [0025], "Programming structures and functionality are implemented in computer-executable instructions as disclosed herein-above for performing steps of the method . . .". Also, "Figure 2 shows a computer system which can be used to implement the present invention", which appears to imply that the invention is not a hardware SOC).

(2) The recited external model ("an external model (i.e., hardware)"), appears to be a software external model because the external model appears to be the verification test bench, which is software as shown in figure 2, element 450.

(3) The recited SOC interface ("SOC interface (i.e., hardware)"), appears to be software because as recited in the specification, "The term "SOC" as used herein refers to combinations of discrete logic blocks, often referred to as "cores" (paragraph [0004]), and "A core may be in the form of a netlist" (paragraph [0005]), and "In its developmental stages, a core is typically embodied as a simulatable HDL model written at some level of abstraction" (paragraph [0005]).

(4) The recited external bus interface ("external bus interface unit (i.e., hardware)"), appears to be software because it is part of the verification test bench, which is software as shown in figure 2, element 450.

The Applicant asserts that the SOC is hardware, but as discussed above, the SOC at least has an interpretation as software. Further, the invention appears to be directed entirely to a software SOC; please see paragraph [0025] which recites, "Figure 2 shows a computer system which can be used to implement the present invention", which appears to imply that the invention is not a hardware SOC, since the invention is implemented on a computer with a simulator.

Further, it was common knowledge in the art to extract timing from floor plans and back annotate the HDL to account for timing in the HDL simulation.

The entire specification is considered to apply to the claims, at least because paragraph [0025] recites, "Figure 2 shows a computer system which can be used to implement the present invention", which appears to include figure 1. Further, the interpretation of an SOC in figure 1 is influenced by the recited, "The term "SOC" as used herein refers to combinations of discrete logic blocks, often referred to as "cores" (paragraph [0004]), and "A core may be in the form of a netlist" (paragraph [0005]), and "In its developmental stages, a core is typically embodied as a simulatable HDL model written at some level of abstraction" (paragraph [0005]).

Paragraph [0004] recites, "The term "SOC" as used herein". The term "herein" appears to refer to the entire specification. Thus, paragraph [0004] and its related support in the other paragraphs appear to refer to the invention.

Regarding claims 2, 8-27 rejected under 35 U.S.C. § 112, first paragraph:

Applicant's arguments appear to be essentially the same as those used for the rejection above under 35 U.S.C. § 112, first paragraph, and thus the Examiner replies as recited above.

Regarding claims 2 and 8 - 34 rejected under 35 USC § 101:

Applicant's arguments appear to be essentially the same as those used for the rejection above under 35 U.S.C. § 112, first paragraph, and thus the Examiner replies as recited above.

Thus, as discussed above, the rejections are maintained.

